PAT-NO: JP407226485A

DOCUMENT-IDENTIFIER: JP 07226485 A

TITLE: MANUFACTURING METHOD OF **CAPACITOR** FOR INTEGRATED CIRCUIT

PUBN-DATE: August 22, 1995

INVENTOR-INFORMATION:
NAME
HIROSE, TATSUYA

ASSIGNEE-INFORMATION:

NAME	COUNTRY
FUJITSU LTD	N/A

APPL-NO: JP06016029

APPL-DATE: February 10, 1994

INT-CL (IPC): H01L027/04, H01L021/822

ABSTRACT:

PURPOSE: To enable a large **capacitor** in thin film to be manufactured at low temperature for realizing the on chip **capacitor**.

CONSTITUTION: A lower electrode 13 comprising **Ti** is formed on a protective film 12 comprising SiON covering a substrate 11 and then a high dielectric film 14 comprising **TiO**<SB>2</SB> required of high temperature baking step is formed at a low temperature having conductivity, next, the surface of the high dielectric film 14 is heated at a baking temperature by irradiating with the beams from a heavy hydrogen lamp having the wavelength in a region in shorter

intrusion length than the film thickness of the high did dielectric film 14 and
low transmittivity to the film 14 i.e., 125 (nm) and 160(nm) so as to form
extremely thin high resistant film 14A. Next, the high resistant film 14A is
used as a substantial dielectric film of a **capacitor** thereby enabling compact
and large capacity **capacitor** to be manufactured at low temperature.